What is claimed is:

1. A semiconductor processing device being capable of inputting/outputting encrypted data from/to an outside and being formed over a semiconductor substrate comprising:

a first non-volatile memory for erasing stored information on a first data length unit;

a second non-volatile memory for erasing stored information on a second data length unit; and

a central processing unit,

wherein the first non-volatile memory is used for storing an encryption key to be used for encrypting the data,

the second non-volatile memory is used for storing a program to be processed by the central processing unit,

each of the first non-volatile memory and the second non-volatile memory has a plurality of non-volatile memory cells,

each of the non-volatile memory cells has a channel region between a first diffusion layer region and a second diffusion layer region which are formed on the substrate, has an electric charge storage layer on the channel region through a first insulating film, has a first gate terminal on the electric charge storage layer through a second insulating film, and has a second gate terminal through the first gate terminal and a third insulating film on a second channel region which is adjacent to a first channel region provided under the electric charge

storage layer,

a hot electron generated in the channel region provided under the third insulating film is injected into the electric charge storage layer or an electric charge is extracted from the electric charge storage layer, thereby carrying out an operation for changing a threshold voltage of the memory cell,

the first non-volatile memory has a first control signal line, first gate terminals of a predetermined number of non-volatile memory cells constituting the first non-volatile memory and the first control signal line can be electrically connected to each other, and the first control signal line is connected to the first gate terminals of the predetermined number of non-volatile memory cells through a switch circuit on the first data length unit, and

the second non-volatile memory has a second control signal line, and first gate terminals of a predetermined number of non-volatile memory cells constituting the second non-volatile memory and the second control signal line are electrically connected to each other.

2. The semiconductor processing device according to claim 1, wherein the first non-volatile memory is further used for storing information to be utilized for specifying an individual.

3. The semiconductor processing device according to claim 2, wherein the first data length is smaller than the second data length.

4. The semiconductor processing device according to claim 3, further comprising a terminal to be used for an input/output from/to an outside,

the program being supplied from the outside through the terminal and stored in the second non-volatile memory.

5. The semiconductor processing device according to claim 4, wherein the central processing unit can give access to the first non-volatile memory and the second non-volatile memory in parallel.

6. The semiconductor processing device according to claim 5, wherein the first non-volatile memory has a memory array portion constituted by a plurality of memory cells and a control portion for controlling access to a selected memory cell,

the second non-volatile memory has a memory array portion constituted by a plurality of memory cells and a control portion for controlling access to a selected memory cell, and

the control portion of the first non-volatile memory and the control portion of the second non-volatile memory are common at least partially.

7. The semiconductor processing device according to claim 6, wherein a part of the control portion to be common is an amplifier circuit to be used for amplifying a read signal when data are to be read from a memory cell.

8. The semiconductor processing device according to claim 6, wherein a part of the control portion to be common is a voltage

generating circuit for generating a voltage to be applied to a memory cell when access is to be given to the memory cell.

9. The semiconductor processing device according to claim 6, wherein a part of the control portion to be common is a decoder circuit for selecting a memory cell when access is to be given to the memory cell.

10. An IC card being enclosed with a synthetic resin comprising:

a first non-volatile memory for erasing stored information on a first data length unit;

a second non-volatile memory for erasing stored information on a second data length unit;

a central processing unit; and

a terminal for inputting/outputting data from/to an outside,

wherein encrypted data are input/output from/to the outside,

the first non-volatile memory is used for storing an encryption key to be utilized for encrypting the data,

the second non-volatile memory is used for storing a program to be processed by the central processing unit,

each of the first non-volatile memory and the second non-volatile memory has a plurality of non-volatile memory cells,

each of the non-volatile memory cells has a channel region

between a first diffusion layer region and a second diffusion layer region which are formed on the substrate, has an electric charge storage layer on the channel region through a first insulating film, has a first gate terminal on the electric charge storage layer through a second insulating film, and has a second gate terminal through the first gate terminal and a third insulating film on a second channel region which is adjacent to a first channel region provided under the electric charge storage layer,

a hot electron generated in the channel region provided under the third insulating film is injected into the electric charge storage layer or an electric charge is extracted from the electric charge storage layer, thereby carrying out an operation for changing a threshold voltage of the memory cell,

the first non-volatile memory has a first control signal line, first gate terminals of a predetermined number of non-volatile memory cells constituting the first non-volatile memory and the first control signal line can be electrically connected to each other, and the first control signal line is connected to the first gate terminals of the predetermined number of non-volatile memory cells through a switch circuit on the first data length unit, and

the second non-volatile memory has a second control signal line, and first gate terminals of a predetermined number of non-volatile memory cells constituting the second non-volatile

memory and the second control signal line are electrically connected to each other.

11. An IC card being enclosed with a synthetic resin comprising:

a first non-volatile memory for erasing stored information on a first data length unit;

a second non-volatile memory for erasing stored information on a second data length unit;

a central processing unit; and

an antenna for inputting/outputting data from/to an outside,

wherein encrypted data are input/output from/to the outside,

the first non-volatile memory is used for storing an encryption key to be utilized for encrypting the data,

the second non-volatile memory is used for storing a program to be processed by the central processing unit,

each of the first non-volatile memory and the second non-volatile memory has a plurality of non-volatile memory cells,

each of the non-volatile memory cells has a channel region between a first diffusion layer region and a second diffusion layer region which are formed on the substrate, has an electric charge storage layer on the channel region through a first insulating film, has a first gate terminal on the electric charge

storage layer through a second insulating film, and has a second gate terminal through the first gate terminal and a third insulating film on a second channel region which is adjacent to a first channel region provided under the electric charge storage layer,

a hot electron generated in the channel region provided under the third insulating film is injected into the electric charge storage layer or an electric charge is extracted from the electric charge storage layer, thereby carrying out an operation for changing a threshold voltage of the memory cell,

the first non-volatile memory has a first control signal line, first gate terminals of a predetermined number of non-volatile memory cells constituting the first non-volatile memory and the first control signal line can be electrically connected to each other, and the first control signal line is connected to the first gate terminals of the predetermined number of non-volatile memory cells through a switch circuit on the first data length unit, and

the second non-volatile memory has a second control signal line, and first gate terminals of a predetermined number of non-volatile memory cells constituting the second non-volatile memory and the second control signal line are electrically connected to each other.

12. The IC card according to claim 10 or 11, wherein the central processing unit and the first non-volatile memory are formed

on a first semiconductor substrate,

the second non-volatile memory is formed on a second semiconductor substrate, and

the first non-volatile memory uses a nitride film for a memory cell in order to store data.

13. The IC card according to claim 10 or 11, wherein the central processing unit and the first non-volatile memory are formed on a first semiconductor substrate,

the second non-volatile memory is formed on a second semiconductor substrate, and

the second non-volatile memory uses a floating gate for a memory cell in order to store data.

14. A semiconductor processing device being capable of inputting/outputting encrypted data to/from an outside comprising:

a first non-volatile memory for erasing stored information on a first data length unit;

a second non-volatile memory for erasing stored information on a second data length unit; and

a central processing unit,

wherein each of the first non-volatile memory and the second non-volatile memory has a plurality of memory cells,

each of the memory cells has a source region, a drain region and a channel region between the source region and the drain region, has a data storage insulating layer and a first

gate on the channel region through an insulating layer, and has a second gate on the data storage insulating layer,

each of the first non-volatile memory and the second non-volatile memory has a plurality of first word lines, corresponding memory cells are connected to the first word lines when the stored information is erased from the first non-volatile memory, corresponding memory cells are connected to the first word lines when the stored information is erased from the second non-volatile memory, and the number of the memory cells to be connected to the first word lines in the first non-volatile memory is smaller than that of the memory cells to be connected to the first word lines in the second non-volatile memory,

the first non-volatile memory has the first word lines and the second gates of a predetermined number of memory cells constituting the first non-volatile memory which can be electrically connected to each other, and the first word lines are connected to the second gates of the predetermined number of memory cells through a switch circuit on the first data length unit, and

the second non-volatile memory has the first word lines and the second gates of a predetermined number of memory cells constituting the second non-volatile memory which are electrically connected to each other.

15. The semiconductor processing device according to claim 14, further comprising the same number of second word lines

as that of the first word lines,

the first word line being connected to the second gate of each of the memory cells and the second word line being connected to the first gate of each of the memory cells.

16. The semiconductor processing device according to claim 15, further comprising a switch unit capable of connecting the second gate of a part of the memory cells to be an erasing object of stored information to the first word line when erasing the stored information in the first non-volatile memory.

17. The semiconductor processing device according to claim 16, wherein the switch unit is an MOS transistor of the same conductive type as the non-volatile memory cell.

18. A semiconductor processing device comprising:

a first non-volatile memory for erasing stored information on a first data length unit;

a second non-volatile memory for erasing stored information on a second data length unit;

a central processing unit; and

an external interface circuit,

wherein the first non-volatile memory is used for storing data,

the second non-volatile memory is used for storing a program to be processed by the central processing unit,

each of the first non-volatile memory and the second non-volatile memory has a plurality of non-volatile memory

cells,

each of the non-volatile memory cells has a channel region between a first diffusion layer region and a second diffusion layer region which are formed on the substrate, has an electric charge storage layer on the channel region through a first insulating film, has a first gate terminal on the electric charge storage layer through a second insulating film, and has a second gate terminal through the first gate terminal and a third insulating film on a second channel region which is adjacent to a first channel region provided under the electric charge storage layer,

a hot electron generated in the channel region provided under the third insulating film is injected into the electric charge storage layer or an electric charge is extracted from the electric charge storage layer, thereby carrying out an operation for changing a threshold voltage of the memory cell,

the first data length is smaller than the second data length,

the first non-volatile memory has a first control signal line, first gate terminals of a predetermined number of non-volatile memory cells constituting the first non-volatile memory and the first control signal line can be electrically connected to each other, and the first control signal line is connected to the first gate terminals of the predetermined number of non-volatile memory cells through a switch circuit on the

first data length unit, and

the second non-volatile memory has a second control signal line, and first gate terminals of a predetermined number of non-volatile memory cells constituting the second non-volatile memory and the second control signal line are electrically connected to each other.

19. The semiconductor processing device according to claim 18, wherein the non-volatile memory cell has a source region, a drain region, and a channel region interposed between the source region and the drain region on a semiconductor substrate, a control gate electrode provided through a first insulating film and a memory gate electrode provided through a second insulating film and an electric charge storage insulating film and isolated electrically from the control gate electrode are provided on the channel region, and a gate breakdown voltage of the control gate electrode is lower than that of the memory gate electrode.

20. The semiconductor processing device according to claim 19, wherein the gate breakdown voltage of the control gate electrode is equal to that of an MOS transistor included in the CPU.

21. The semiconductor processing device according to claim 19, wherein the first non-volatile memory holds, on the first data length unit, information in a memory cell from which stored information is erased on the first data length unit.

22. The semiconductor processing device according to claim 19, wherein the second non-volatile memory holds, on a shorter unit than the second data length, information in a memory cell from which stored information is erased on the second data length unit.

23. The semiconductor processing device according to claim 19, wherein the central processing unit can give access to the first non-volatile memory and the second non-volatile memory in parallel.

24. The semiconductor processing device according to claim 23, wherein the first non-volatile memory has a memory array portion constituted by a plurality of memory cells and a control portion for controlling access to a selected memory cell,

the second non-volatile memory has a memory array portion constituted by a plurality of memory cells and a control portion for controlling access to a selected memory cell, and

the control portion of the first non-volatile memory and the control portion of the second non-volatile memory are common at least partially.

25. The semiconductor processing device according to claim 24, wherein a part of the control portion to be common is an amplifier circuit to be used for amplifying a read signal when data are to be read from a memory cell.

26. The semiconductor processing device according to claim 24, wherein a part of the control portion to be common is a

voltage generating circuit for generating a voltage to be applied to a memory cell when access is to be given to the memory cell.

27. The semiconductor processing device according to claim 24, wherein a part of the control portion to be common is a decoder circuit for selecting a memory cell when access is to be given to the memory cell.

28. An IC card being enclosed with a synthetic resin comprising:

a first non-volatile memory for erasing stored information on a first data length unit;

a second non-volatile memory for erasing stored information on a second data length unit;

a central processing unit; and

a terminal for inputting/outputting data from/to an outside,

wherein the first non-volatile memory is used for storing data,

the second non-volatile memory is used for storing a program to be processed by the central processing unit,

each of the first non-volatile memory and the second non-volatile memory has a plurality of non-volatile memory cells,

each of the non-volatile memory cells has a channel region between a first diffusion layer region and a second diffusion layer region which are formed on the substrate, has an electric

charge storage layer on the channel region through a first insulating film, has a first gate terminal on the electric charge storage layer through a second insulating film, and has a second gate terminal through the first gate terminal and a third insulating film on a second channel region which is adjacent to a first channel region provided under the electric charge storage layer,

a hot electron generated in the channel region provided under the third insulating film is injected into the electric charge storage layer or an electric charge is extracted from the electric charge storage layer, thereby carrying out an operation for changing a threshold voltage of the memory cell,

the first data length is smaller than the second data length,

the first non-volatile memory has a first control signal line, first gate terminals of a predetermined number of non-volatile memory cells constituting the first non-volatile memory and the first control signal line can be electrically connected to each other, and the first control signal line is connected to the first gate terminals of the predetermined number of non-volatile memory cells through a switch circuit on the first data length unit, and

the second non-volatile memory has a second control signal line, and first gate terminals of a predetermined number of non-volatile memory cells constituting the second non-volatile

memory and the second control signal line are electrically connected to each other.

29. An IC card comprising a first non-volatile memory for erasing stored information on a first data length unit, a second non-volatile memory for erasing stored information on a second data length unit, a central processing unit, and an antenna for inputting/outputting data from/to an outside which are enclosed with a synthetic resin,

wherein the first non-volatile memory is used for storing data,

the second non-volatile memory is used for storing a program to be processed by the central processing unit,

each of the first non-volatile memory and the second non-volatile memory has a plurality of non-volatile memory cells,

each of the non-volatile memory cells has a channel region between a first diffusion layer region and a second diffusion layer region which are formed on the substrate, has an electric charge storage layer on the channel region through a first insulating film, has a first gate terminal on the electric charge storage layer through a second insulating film, and has a second gate terminal through the first gate terminal and a third insulating film on a second channel region which is adjacent to a first channel region provided under the electric charge storage layer,

a hot electron generated in the channel region provided under the third insulating film is injected into the electric charge storage layer or an electric charge is extracted from the electric charge storage layer, thereby carrying out an operation for changing a threshold voltage of the memory cell,

the first data length is smaller than the second data length,

the first non-volatile memory has a first control signal line, first gate terminals of a predetermined number of non-volatile memory cells constituting the first non-volatile memory and the first control signal line can be electrically connected to each other, and the first control signal line is connected to the first gate terminals of the predetermined number of non-volatile memory cells through a switch circuit on the first data length unit, and

the second non-volatile memory has a second control signal line, and first gate terminals of a predetermined number of non-volatile memory cells constituting the second non-volatile memory and the second control signal line are electrically connected to each other.

30. The semiconductor processing device according to claim 28 or 29, wherein the non-volatile memory cell has a source region, a drain region, and a channel region interposed between the source region and the drain region on a semiconductor substrate, a control gate electrode provided through a first

insulating film and a memory gate electrode provided through a second insulating film and an electric charge storage insulating film and isolated electrically from the control gate electrode are provided on the channel region, and a gate breakdown voltage of the control gate electrode is lower than that of the memory gate electrode.

31. The semiconductor processing device according to claim 30, wherein the gate breakdown voltage of the control gate electrode is equal to that of an MOS transistor included in the CPU.